REMARKS

Claims 17-40 are all the claims pending in the application.

I. Objection to the Specification and Claim Rejections under 35 U.S.C. § 112, first paragraph

The specification has been objected to because the Examiner has indicated that there is insufficient antecedent basis for the phrase "before being deinterleaved" as used in the claims. In a similar manner, claims 17-40 have been rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement because the Examiner has indicated that the phrase "before being deinterleaved" as used in the claims was not described in such a way as to reasonably convey to one skilled in the art that the inventors, at the time the application was filed, had possession of the claimed invention.

By this amendment, Applicants note that the specification has been amended so as to incorporate the phrase "before being deinterleaved" therein. In particular, Applicants note that the specification has been amended to recite the following: "Since, before being deinterleaved, the main data between sub data or the main data between sub data and SY have the same erasure position information, erasure position information should be set at only the boundary between the main data area and the sub data area or the SY area" (see page 16, lines 11-15 of the substitute specification).

Based on the foregoing amendment to the specification, Applicants respectfully submit that the specification now provides explicit antecedent basis for the phrase "before being deinterleaved".

Furthermore, Applicants respectfully submit that the use of the phrase "before being deinterleaved" in the specification is not new matter, and that the use of this phrase in the claims satisfies the written description requirement because one of ordinary skill in the art would have understood the disclosure as originally filed to implicitly provide support for such a feature.

In particular, Applicants note that the specification describes that the data in the ECC block is in an interleaved state, with main data of the ECC block that is located between the same bytes of sub data having the same erasure position information (e.g., see Fig. 4(b)), that this

interleaved data is rearranged in an error correction order, and error correction is then performed utilizing the erasure position information (e.g., see Figs. 7 and 8, and the corresponding description in the specification at pages 20-24).

In this regard, with respect to Figs. 7 and 8 of the present application, Applicants note that the numerical values shown in the code lines therein make it clear that data of the ECC block as shown in Fig. 4b (i.e., the data in the interleaved state, or in other words, before being deinterleaved) is deinterleaved prior to error correction being performed (e.g., see the corresponding description of Figs. 7 and 8 on pages 20-24 of the specification). Accordingly, Applicants submit that the use of the phrase "before being deinterleaved", while not expressly utilized in the original specification, has implicit support in the original specification.

Applicants note that the MPEP indicates that in order to comply with the written description requirement..., each claim limitation must be expressly, implicitly, or inherently supported in the originally filed disclosure" (emphasis added) (see MPEP 2163(II)(A)(3)(b)). Accordingly, while the specification as originally filed did not expressly utilize the phrase "before being deinterleaved", for the reasons discussed above, Applicants respectfully submit that such a feature is implicitly supported by the originally filed disclosure, and therefore, that one of ordinary skill in the art would have understood, at the time the patent application was filed, that the description requires such a feature.

In view of the foregoing, Applicants respectfully submit that the phrase "before being deinterleaved" meets the written description requirement of 35 U.S.C. 112, first paragraph. Therefore, Applicants kindly request that the above-noted rejection be reconsidered and withdrawn.

II. Objections to the Claims

A. Claims 19, 24, 37 and 38 have been objected to as being of improper dependent form for failing to further limit the subject matter of a previous claim. In particular, the Examiner has indicated that the claims fail to recite any positive limitation further limiting the error correction methods recited in claims 18 and 23.

Regarding the Examiner's position, Applicants note that there is no requirement that

dependent claims recite active method steps, and furthermore, point out that MPEP 608.01(n)(III) clearly sets forth that the "test as to whether a claim is a proper dependent claim is that it shall include every limitation of the claim from which it depends (35 U.S.C. 112, fourth paragraph) or in other words that it shall not conceivably be infringed by anything which would not also infringe the basic claim."

Even though Applicants disagree with the Examiner's objection for the reasons set forth above, in an effort to expedite prosecution, Applicants have amended claims 19, 24, 37 and 38 such that these claims are now in independent form. In view of the foregoing, Applicants kindly request that the above-noted objection be reconsidered and withdrawn.

B. Claims 29-31, 39, 34-36 and 40 have been objected to as being of improper dependent form for failing to further limit the subject matter of a previous claim. In particular, the Examiner has indicated that the claims fail to recite any structural limitations that further limit the error correction apparatus recited in claims 28 and 33.

Regarding the Examiner's position, Applicants note that there is no requirement that dependent claims recite structural limitations, and furthermore, point out that MPEP 608.01(n)(III) clearly sets forth that the "test as to whether a claim is a proper dependent claim is that it shall include every limitation of the claim from which it depends (35 U.S.C. 112, fourth paragraph) or in other words that it shall not conceivably be infringed by anything which would not also infringe the basic claim."

Even though Applicants disagree with the Examiner's objection for the reasons set forth above, in an effort to expedite prosecution, Applicants have amended claims 29-31, 39, 34-36 and 40 such that these claims are now in independent form. In view of the foregoing, Applicants kindly request that the above-noted objection be reconsidered and withdrawn.

III. Claim Rejections under 35 U.S.C. § 112, second paragraph

A. Claims 18, 19, 23, 24, 37 and 38 have been rejected under 35 U.S.C. § 112, second paragraph as being incomplete for omitting essential steps, such omission amounting to a gap between the steps.

Regarding the above-noted rejection, with respect to claims 18 and 23, the Examiner has indicated that the features recited therein drawn to the description of the ECC block (e.g., the "main data area" and the "sub data areas" of the ECC block) is "non-functional descriptive material" that fails to recite any functional steps of a method explicitly relating the "non-functional descriptive material" to the error correction methods of claims 18 and 23, and therefore, that the claims are rendered indefinite. Applicants respectfully disagree.

First, Applicants note that there is no requirement that all features recited in a method claim be active method steps in order to satisfy the requirements of 35 U.S.C. 112, second paragraph. If the Examiner disagrees, and believes that every feature in a method claim must be an active method step in order to satisfy the requirements of 35 U.S.C. 112, second paragraph, then Applicants kindly request that the Examiner identify the section of the MPEP which supports such a position.

In this regard, contrary to the position taken by the Examiner, Applicants point out that the MPEP explicitly states that "Applicant may use functional language, alternative expressions, negative limitations, or any style of expression or format of claim which makes clear the boundaries of the subject matter for which protection is sought" (emphasis added) (see MPEP 2173.01). Further, Applicants note that MPEP 2173.01 also states that "a claim may not be rejected solely because of the type of language used to define the subject matter for which protection is sought" (emphasis added).

Taking the foregoing into account, Applicants respectfully submit that the features recited in claims 18 and 23 drawn to the description of the ECC block are clear and precise, and make clear the boundaries of the subject matter for which protection is sought. Further, regarding the Examiner's position that such features do not relate to the error correction methods described therein, Applicants respectfully disagree. In particular, Applicants point out that the description of the ECC block in claims 18 and 23 is used to further define the steps of "configuring erasure position of said first byte of main data belonging to the error correction target code line..." and "performing error correction on the error correction target code line" by clearly defining the location of the error correction target code line within the ECC block, namely, by reciting in claims 18 and 23 that "said error correction target code line extends so as to be located in both of

the first and second main data areas of the ECC block before being deinterleaved".

With respect to claims 19, 24, 37 and 38, the Examiner has indicated that these claims fail to recite any positive limitation further limiting the error correction methods of claims 18 and 23, but instead, recite the intended use of the error correction methods of claims 18 and 23 without reciting any positive method steps.

Regarding the Examiner's position, Applicants initially note that claims 19, 24, 37 and 38 have been rewritten in independent form in order to expedite prosecution. Further, as noted above, Applicants point out that the MPEP explicitly states that "Applicant may use functional language, alternative expressions, negative limitations, or any style of expression or format of claim which makes clear the boundaries of the subject matter for which protection is sought" (emphasis added) (see MPEP 2173.01). Further, Applicants note that MPEP 2173.01 also states that "a claim may not be rejected solely because of the type of language used to define the subject matter for which protection is sought" (emphasis added).

Taking the foregoing into account, Applicants respectfully submit that the features recited in claims 19, 24, 37 and 38 are clear and precise, and make clear the boundaries of the subject matter for which protection is sought. Further, regarding the Examiner's position that such features do not further define the error correction methods described therein, Applicants respectfully disagree. In particular, Applicants note that the feature recited therein which recites that "wherein said configuring erasure position information on said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals" further defines the "configuring erasure position information" step recited therein because it clearly requires that the claimed step utilize "sync data that is located in the ECC block at predetermined intervals."

In view of the foregoing, Applicants respectfully submit that claims 18, 19, 23, 24, 37 and 38 meet the requirements of 35 U.S.C. 112, second paragraph, and therefore, kindly request that the rejection be reconsidered and withdrawn.

Lastly, with respect to the requirements of 35 U.S.C. 112, second paragraph, Applicants note that the MPEP indicates that the "Examiner's focus during examination of the claims for compliance with the requirement for definiteness of 35 U.S.C. 112, second paragraph, is whether the claim meets the threshold requirements of clarity and precision, not whether more suitable

language of modes of expression are available" (emphasis added) (see MPEP 2173.02). Further, Applicants note that MPEP 2173.02 also indicates that "[s]ome latitude in the manner of expression and the aptness of terms should be permitted even though the claim language is not as precise as the examiner might desires", and that "Examiners are encouraged to suggest claim language to applicants to improve the clarity and precision of the language used, but should not reject claims or insist on their own preferences if other modes of expression selected by applicants satisfy the statutory requirements".

In view of the foregoing, Applicants kindly request that the rejection of the claims under 35 U.S.C. 112, second paragraph be reconsidered and withdrawn.

B. Claims 28 and 33 have been rejected under 35 U.S.C. § 112, second paragraph as being incomplete for omitting essential steps, such omission amounting to a gap between the steps.

Regarding the above-noted rejection of claims 28 and 33 (which are apparatus claims), the Examiner has essentially taken the same position as described above in connection with method claims 18 and 23, but has indicated that claims 28 and 33 fail to recite any structural element relating to the description of the ECC block (e.g., the "main data area" and the "sub data areas" of the ECC block) to to the error correction apparatus of claims 28 and 33. For at least similar reasons as discussed above, Applicants respectfully disagree.

First, Applicants note that there is no requirement that all features recited in an apparatus claim be structural elements in order to satisfy the requirements of 35 U.S.C. 112, second paragraph. If the Examiner disagrees, and believes that every feature in an apparatus claim must be a positively recited structural element in order to satisfy the requirements of 35 U.S.C. 112, second paragraph, then Applicants kindly request that the Examiner identify the section of the MPEP which supports such a position.

In this regard, contrary to the position taken by the Examiner, Applicants point out that the MPEP explicitly states that "Applicant may use functional language, alternative expressions, negative limitations, or any style of expression or format of claim which makes clear the boundaries of the subject matter for which protection is sought" (emphasis added) (see MPEP

2173.01). Further, Applicants note that MPEP 2173.01 also states that "a claim may not be rejected solely because of the type of language used to define the subject matter for which protection is sought" (emphasis added).

Taking the foregoing into account, Applicants respectfully submit that the features recited in claims 28 and 33 drawn to the description of the ECC block are clear and precise, and make clear the boundaries of the subject matter for which protection is sought. Further, regarding the Examiner's position that such features do not relate to the error correction apparatus described therein, Applicants respectfully disagree. In particular, Applicants point out that the description of the ECC block in claims 28 and 33 is used to further define the features of "a configuring means for configuring erasure position of said first byte of main data belonging to the error correction target code line..." and "an error correction means for performing error correction on the error correction target code line" by clearly defining the location of the error correction target code line within the ECC block, namely, by reciting in claims 28 and 33 that "said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block before being deinterleaved".

In view of the foregoing, Applicants respectfully submit that claims 28 and 33 meet the requirements of 35 U.S.C. 112, second paragraph, and therefore, kindly request that the rejection be reconsidered and withdrawn.

Further, with respect to the requirements of 35 U.S.C. 112, second paragraph, as pointed out above, Applicants note that the MPEP indicates that the "Examiner's focus during examination of the claims for compliance with the requirement for definiteness of 35 U.S.C. 112, second paragraph, is whether the claim meets the threshold requirements of clarity and precision, not whether more suitable language of modes of expression are available" (emphasis added) (see MPEP 2173.02). Further, Applicants note that MPEP 2173.02 also indicates that "[s]ome latitude in the manner of expression and the aptness of terms should be permitted even though the claim language is not as precise as the examiner might desires", and that "Examiners are encouraged to suggest claim language to applicants to improve the clarity and precision of the language used, but should not reject claims or insist on their own preferences if other modes of expression selected by applicants satisfy the statutory requirements".

In view of the foregoing, Applicants kindly request that the rejection of the claims under 35 U.S.C. 112, second paragraph be reconsidered and withdrawn.

IV. Claim Rejections under 35 U.S.C. § 102/103

Claims 17, 19, 20, 22, 24, 25, 27, 29, 30, 32, 34 and 35 have been rejected under 35 U.S.C. § 102(b) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as being obvious over Marchant (US 6,631,492) and Kobayashi et al. (US 6,029,264).

Initially, regarding the above-noted rejection, Applicants note that it is somewhat unclear how the Examiner is relying on each of the applied references in formulating the rejection. In particular, Applicants note that is not fully clear if the Examiner is taking the position that (1) the above-noted claims are being rejected as being anticipated by Marchant, or in the alternative, as being obvious over Marchant in view of Kobayashi, or (2) the above-noted claims are being rejected as being anticipated by either Marchant or Kobayashi, or in the alternative, as being obvious over Marchant or Kobayashi. Clarification is kindly requested.

Regarding claim 17, Applicants note that this claim recites the features of judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved; and configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved.

Applicants respectfully submit that Marchant and Kobayashi, either alone or in combination, do not disclose, suggest or otherwise render obvious at least the above-noted features recited in claim 17.

In particular, with respect to the disclosure at col. 6, lines 28-56 of Marchant, which the Examiner has relied on in the Office Action (see pages 10-11), Applicants note that this

disclosure relates to Fig. 7 of Marchant, which depicts a block of transverse ECC code word symbols 36' recorded on a band of longitudinal data tracks 24', with scratch detection fields 44a and 44b being recorded at each end of the block (see col. 6, lines 30-32).

As disclosed in Marchant, scratch detection occurs when a positional coincidence is found between defective scratch detection symbols 48a and 48b in consecutive scratch detection fields, with the sections of data tracks connecting such defective scratch detection symbols 48a and 48b being flagged as suspect scratch locations (see col. 6, lines 40-44). In this regard, as explained in Marchant, all transverse ECC code word symbols 36' that are disposed on the flagged data track segments may then be processed by erasure correction (see col. 6, lines 40-44).

In the Office Action, the Examiner has taken the position that the scratch detection fields 48a, 48b of Fig. 7 of Marchant correspond to the bytes of main data, and has also asserted that "Marchant teaches an embodiment where scratch detection takes place before de-interleaving on read Cross-interleaved ECC encoded data" (See Office Action at page 11). Thus, the Examiner appears to be taking the position that the data shown in Fig. 7 of Marchant is cross-interleaved data. Applicants respectfully disagree.

First, with respect to the disclosure in Marchant at col. 4, lines 41-60, which discusses cross interleaved codes, Applicants note that this disclosure is not directed to Fig. 7, but instead, is directed to Fig. 4 of Marchant, which is a "prior art" figure. Second, with respect to the disclosure at col. 5, lines 40-42 of Marchant, which indicates that "the band of data tracks on which a transverse ECC code word is recorded may interleaved in the cross track direction with one or more other bands of data tracks", Applicants note that this description is also not directed to Fig. 7 of Marchant, but instead, is directed to Fig. 5.

In this regard, while Figs. 4 and 5 of Marchant utilize data that is interleaved in the cross-track direction, Applicants respectfully submit that in Fig. 7, the defective scratch detection symbols 48a and 48b, as well as the ECC code word symbols 36', are not interleaved. If the Examiner disagrees, and believes that the data in Fig. 7 of Marchant is interleaved, Applicants kindly request that the Examiner provide support for such a position.

To the extent that the Examiner takes the position that it would have been obvious to utilize the cross-interleaved data as described in Marchant (i.e., in the description of Figs. 4 and

5) as the data shown in Fig. 7, Applicants respectfully submit that such a position is incorrect.

In particular, Applicants note that if cross-interleaved data was utilized in Fig. 7, that it would be impossible to determine the correct position where a scratch has occurred. The reason for this is as follows.

As is evident from Fig. 7 of Marchant, when performing error correction, in order to determine the correction position where a scratch has occurred, it would be necessary to perform error correction on areas of the **same track**. Thus, if the data shown in Fig. 7 of Marchant was interleaved in a **cross-track** direction, Applicants note that it would simply not be possible to determine the correct location of the scratch because the error correction would not be able to be performed on areas of the **same track**.

In view of the foregoing, Applicants respectfully submit that Marchant does not disclose or suggest the above-noted features recited in claim 17 of judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved; and configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved.

Regarding Kobayashi, Applicants note that this reference discloses a process of adding an erasure flag before deinterleaving is performed. With respect to such disclosure, however, Applicants note that such disclosure merely refers to the well known process of adding a flag and later utilizing the flag to perform erasure correction. Applicants respectfully submit that such disclosure, even if considered in combination with the disclosure in Marchant, would not suggest or render obvious the above-noted features recited in claim 17 of judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data

before being deinterleaved; and configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved.

Moreover, to the extent that the Examiner is taking the position that the erasure flags of Kobayashi correspond to the "erasure position information" as recited in claim 17, Applicants respectfully disagree.

In particular, Applicants note that the erasure flags of Kobayashi are merely utilized to identify data to which error correction is to be performed, whereas the "erasure position information" recited in claim 17 is described as being configured to be identical for first and second bytes of main data when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved.

In other words, Applicants note that because the erasure flags of Kobayashi will clearly not be "configured" as set forth above in claim 17 (i.e., claim 17 recites the feature of configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved), Applicants respectfully submit that the erasure flags of Kobayashi do not correspond to the erasure position information as described in claim 17.

In view of the foregoing, Applicants respectfully submit that Marchant and Kobayashi, either considered alone or in combination, do not disclose, suggest or otherwise render obvious at least the above-noted features recited in amended claim 17. Accordingly, Applicants submit that claim 17 is patentable over the cited prior art, an indication of which is kindly requested.

Regarding claim 19, Applicants note that this claim has been rewritten in independent form, and recites the features of judging whether or not a first byte of main data, which is one of

a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved; and configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved.

For at least similar reasons as discussed above with respect to claim 17, Applicants respectfully submit that the above-noted features recited in claim 19 are not disclosed, suggested or otherwise rendered obvious by the cited prior art. Accordingly, Applicants submit that claim 19 is patentable over the cited prior art, an indication of which is kindly requested. Claim 20 depends from claim 19 and is therefore considered patentable at least by virtue of its dependency.

Regarding claims 22 and 24, Applicants note that these claims recite the features of judging whether or not a first byte of data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information; and configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved.

For at least similar reasons as discussed above with respect to claim 17, Applicants respectfully submit that the above-noted features recited in claims 22 and 24 are not disclosed, suggested or otherwise rendered obvious by the cited prior art. Accordingly, Applicants submit that claims 22 and 24 are patentable over the cited prior art, an indication of which is kindly requested. Claim 25 depends from claim 24 and is therefore considered patentable at least by

virtue of its dependency.

Regarding claims 27, 29 and 30, Applicants note that these claims recite the features of a judgment means for judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved; and a configuration means for configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judgment means judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved.

For at least similar reasons as discussed above with respect to claim 17, Applicants respectfully submit that the above-noted features recited in claims 27, 29 and 30 are not disclosed, suggested or otherwise rendered obvious by the cited prior art. Accordingly, Applicants submit that claims 27, 29 and 30 are patentable over the cited prior art, an indication of which is kindly requested.

Regarding claims 32, 34 and 35 Applicants note that these claims recite the features of a judgment means for judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information; and a configuration means for configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judgment means judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved.

For at least similar reasons as discussed above with respect to claim 17, Applicants

respectfully submit that the above-noted features recited in claims 32, 34 and 35 are not disclosed, suggested or otherwise rendered obvious by the cited prior art. Accordingly, Applicants submit that claims 32, 34 and 35 are patentable over the cited prior art, an indication of which is kindly requested.

VI. Claim Rejections under 35 U.S.C. § 103(a)

A. Claims 18, 23, 28, 33 and 37-40 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Marchant (US 6,631,492) and Kobayashi et al. (US 6,029,264) in view of Shutoku et al. (US 7,089,401).

Regarding claims 18 and 37, Applicants note that these claims have been amended to recite the features of judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved; and configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved.

For at least similar reasons as discussed above with respect to claim 17, Applicants respectfully submit that the above-noted features recited in claims 18 and 37 are not disclosed, suggested or otherwise rendered obvious by Marchant and Kobayashi, when either taken alone or in combination. Further, Applicants respectfully submit that Shutoku does not cure these deficiencies of Marchant and Kobayashi. Accordingly, Applicants submit that claims 18 and 37 are patentable over the cited prior art, an indication of which is kindly requested. Claim 40 depends from claim 37 and is therefore considered patentable at least by virtue of its dependency.

Regarding claim 23 and 38, Applicants note that these claims have been amended to recite the features of judging whether or not a first byte of data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one

of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information; and configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved.

For at least similar reasons as discussed above with respect to claim 17, Applicants respectfully submit that the above-noted features recited in claims 23 and 38 are not disclosed, suggested or otherwise rendered obvious by Marchant and Kobayashi, when either taken alone or in combination. Further, Applicants respectfully submit that Shutoku does not cure these deficiencies of Marchant and Kobayashi. Accordingly, Applicants submit that claims 23 and 38 are patentable over the cited prior art, an indication of which is kindly requested.

Regarding claims 28 and 39, Applicants note that these claims have been amended to recite the features of a judgment means for judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved; and a configuration means for configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judgment means judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved.

For at least similar reasons as discussed above with respect to claim 17, Applicants respectfully submit that the above-noted features recited in claims 28 and 39 are not disclosed, suggested or otherwise rendered obvious by Marchant and Kobayashi, when either taken alone or in combination. Further, Applicants respectfully submit that Shutoku does not cure these deficiencies of Marchant and Kobayashi. Accordingly, Applicants submit that claims 28 and 39

patentable over the cited prior art, an indication of which is kindly requested.

Regarding claims 33 and 40, Applicants note that these claims have been amended to recite the features of a judgment means for judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information; and a configuration means for configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judgment means judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved.

For at least similar reasons as discussed above with respect to claim 17, Applicants respectfully submit that the above-noted features recited in claims 33 and 40 are not disclosed, suggested or otherwise rendered obvious by Marchant and Kobayashi, when either taken alone or in combination. Further, Applicants respectfully submit that Shutoku does not cure these deficiencies of Marchant and Kobayashi. Accordingly, Applicants submit that claims 33 and 40 are patentable over the cited prior art, an indication of which is kindly requested.

Regarding claim 37, Applicants note that this claim has been amended to recite the features of a judgment means for judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information; and a configuration means for configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judgment means judges that the first byte of main

data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved.

For at least similar reasons as discussed above with respect to claim 17, Applicants respectfully submit that the above-noted features recited in claim 37 are not disclosed, suggested or otherwise rendered obvious by Marchant and Kobayashi, when either taken alone or in combination. Further, Applicants respectfully submit that Shutoku does not cure these deficiencies of Marchant and Kobayashi. Accordingly, Applicants submit that claim 37 is patentable over the cited prior art, an indication of which is kindly requested.

B. Claims 21, 26, 31 and 36 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Marchant (US 6,631,492) and Kobayashi et al. (US 6,029,264) in view of Eachus (US 3,685,016).

Claim 21 depends from claim 19, and claim 26 depends from claim 24. Applicants respectfully submit that Eachus does not cure the above-noted deficiencies of Marchant and Kobayashi, with respect to claims 19 and 24. Accordingly, Applicants submit that claims 21 and 26 are patentable at least by virtue of their dependency.

Regarding claims 31 and 36, Applicants note that these claims have been rewritten in independent form including all of the features of claims 27 and 32, respectively. For at least similar reasons as discussed above with respect to claim 17, Applicants respectfully submit that Marchant and Kobayashi do not disclose, suggest or otherwise render obvious all of the features recited in claims 31 and 36. Further, Applicants respectfully submit that Eachus does not cure the above-noted deficiencies of Marchant and Kobayashi. Accordingly, Applicants submit that claims 31 and 36 are patentable over the cited prior art, an indication of which is kindly requested.

VII. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited.

If any points remain in issue which the Examiner feels may best be resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Syuji MATSUDA et al.

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